ABSTRACT OF THE INVENTION

The data rate at which DMA transactions are processed by a General Purpose Computer System can be significantly improved by directing housekeeping type transactions directly to the CPU bus and by directing data type

5   transactions directly to Shared Memory. By assigning memory address ranges to particular I/O devices and by programming PCI Interface Logic on a System Controller to detect these ranges and to direct DMA requests directly to either the CPU bus or to the Memory Controller depending upon the address range detected, the speed with which DMA transactions can be processed is enhanced.

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